SUMMER-19 EXAMINATION

Subject Name: Digital Communication System <u>Model Answer</u> Subject Code: 22428

Important Instructions to examiners:

1) The answers should be examined by key words and not as word-to-word as given in themodel answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may tryto assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given moreImportance (Not applicable for subject English and Communication Skills.
4) While assessing figures, examiner may give credit for principal components indicated in thefigure. The figures drawn by candidate and model answer may vary. The examiner may give credit for anyequivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed constantvalues may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgement on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on equivalent concept.

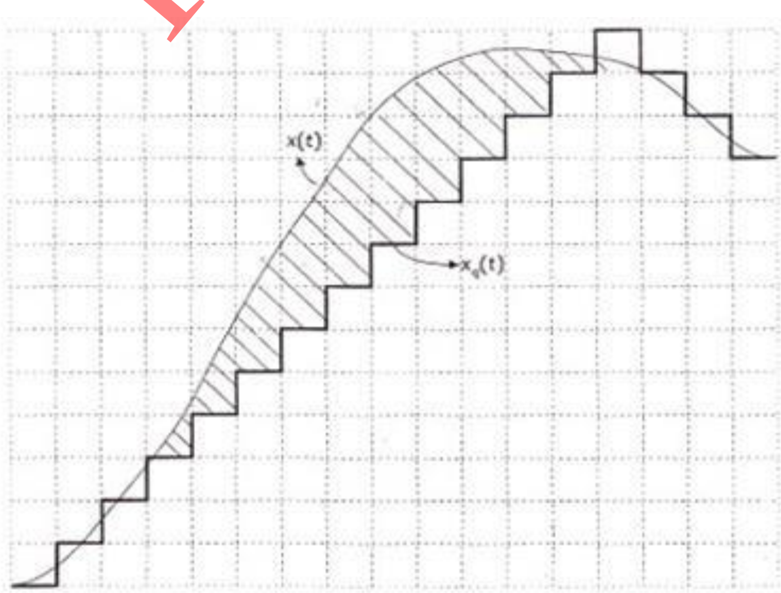
Q. No.	Sub Q. N.	Answers	Marking Scheme
1	(A)	**Attempt any FIVE of the following:**	**10-Total Marks**
	(a)	**State any two advantages and disadvantages of digital communication system.**	**2M**
	Ans:	**Advantages of digital communication** • Digital signals are better suited than analog signals for procession and combining using technique called multiplexing. • Digital transmission systems are more resistant to analog systems to additive noise because they use signal regeneration rather than signal amplification. • Digital signals are simpler to measure and evaluate than analog signals. • In digital systems transmission errors can be corrected and detected more accurately. • Using data encryption only permuted receivers can be allowed to detect the	**Any 2 advantages - 1mark** **Any 2 disadvantages - 1mark**

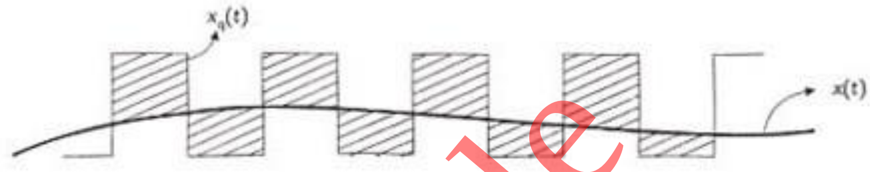
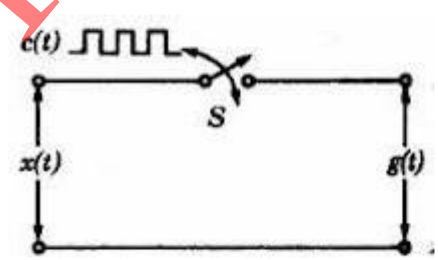
		transmission data. • Wide dynamic range. • Because of the advances of IC technologies and high speed computers, digital communication systems are simpler and cheaper. • Digital communication is adaptive to other advance branches of data processing such as digital. **Disadvantages of Digital Communication** • The transmission of digitally encoded analog signals requires significantly more bandwidth. • Digital transmission requires precise time synchronization between the clocks in the transmitter and receiver.	
	(b)	**State characteristics of communication channel.**	**2M**
	Ans:	**Characteristics of communication channel.** **1. Bit rate** **2.Baud rate** **3.Bandwidth** **4.Repeater distance** **5.Channel capacity**	Any 2 **characteristics 2M**
	(c)	**State sampling theorem.**	**2M**
	Ans:	**Sampling theorem:** Sampling theorem states that a band-limited signal of finite energy having the highest frequency component *fm* Hz can be represented and recovered completely from a set of samples taken at a rate of *fs* samples per second provided that ***fs ≥ 2fm***. Where, fs = sampling frequency fm = maximum frequency of continuous original signal	**2M**

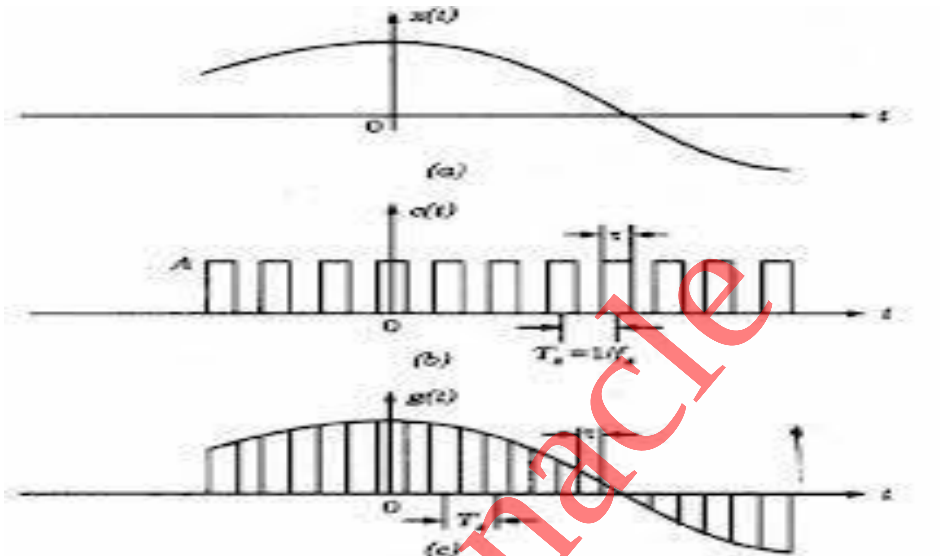
	(d)	**List different digital modulation techniques.**	**2M**
	Ans:	**List of Different Digital Modulation technique:-** (i) Amplitude shift keying -ASK (ii) Phase shift keying - PSK (iii) Frequency shift keying - FSK (iv) Quadrature Phase shift keying - QPSK (v) Differential Phase shift keying -DPSK (vi) Quadrature amplitude modulation- QAM	ANY 4 2M
	e)	**State advantages of TDMA over FDMA**	**2M**
	Ans:	1. In TDMA since only one station is present at any given time so the crosstalk will avoided this is present in FDMA. 2. The entire channel band which can be allocated to signal channel at given instant of time so the data transmission speed is high. 3. TDMA by default can work well with digital; therefore it can be easily used for digital data transmission. 4. In the TDMA since only one station present at any given time, the generation of inter symbol interference will not take place. 5. Due to the absence of intermodulation products, TWT can be operated with maximum power output or saturation level. 6. It is easier to change the capacity between nodes by simply changing the duration and position of each burst in the TDMA frame. It is very flexible. 7. As the transmission is taking place in bursts, its interception by unauthorized elements is difficult. Hence it is more secure than FDMA. 8. Intermodulation products are absent as there is one carrier only in all time slots.	**Any 2 advantages 2M**
	f)	**State the need of multiplexing.**	**2M**
	Ans:	**Need of multiplexing** • In the application like telephony there are large numbers of users involved. It is not possible to lay a separate pair of wires from each subscriber to the other entire subscriber; this is very expensive and practically impossible. • In the Process of multiplexing two or more individual signals are transmitted over a single communication channel. Here we used medium as a coaxial cable or an optical fiber cable because of multiplexing bandwidth utilization is possible.	**2M**

	g)	**State applications of spread spectrum modulation.**	**2M**
	Ans:	1. Jam-resistant communication systems 2. CDMA radios 3. High Resolution Ranging: Spread Specturm Communications is often used in high resolution ranging. It is possible to locate an object with good accuracy using SS techniques. for example where it could be used is Global Positioning System (GPS). 4. WLAN: Wireless LAN (Local Area Networks) widely use spread spectrum communications. i. Infrared (IR) Communications ii. Direct Sequence Spread Spectrum Communications iii. Frequency Hopping Spread Spectrum Communications. 5. Cordless Phones 6. Long-range wireless phones for home and industry 7. Cellular base stations interconnection. 8. Bluetooth.	**Any 2 applications 2M**

Q. No.	Sub Q. N.	.Answers	Marking Scheme
2		**Attempt any THREE of the following:**	**12-Total Marks**
	a)	**State Hartley's law and Shannon Hartley's theorem.**	**4M**
	Ans:	**Hartley's law** The amount of information that can be sent in a given transmission is dependent on the bandwidth of communication channel and the duration of transmission. OR	**2M**

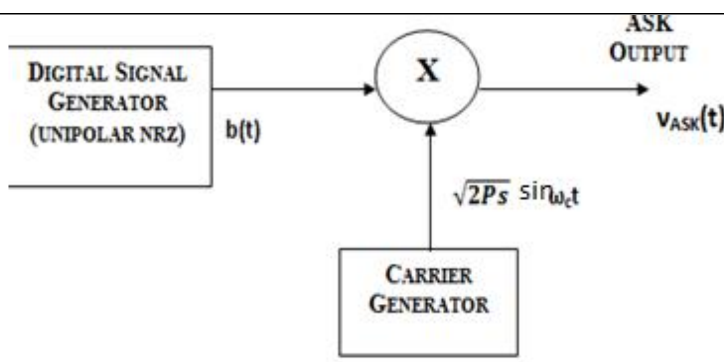
		Hartley's theorem state that if the bandwidth of a transmission channel is "B" which carries a signal having "L" number of levels, then the maximum data rate "R" on this channel is given by : **$R = 2 B \log_2 L$** **Shannon's Hartley theorem:** The channel capacity of a white, band limited Gaussian channel is given by, $$C = B\log_2\left(1+\frac{S}{N}\right)$$ Where, B = Channel Bandwidth S = Signal Power N = Noise within the channel bandwidth	2M
	b)	**Describe slope overload and granular noise in DM system**	4M
	Ans:	**SLOPE-OVERLOAD DISTORTION:** • If the slope of the analog signal $x(t)$ is much higher (steep) than that of the approximated signal $x_q(t)$ over a long duration then $x_q(t)$ will not follow $x(t)$ at all as shown in Figure • The difference between $x(t)$ and $x_q(t)$ is called the ***slope-overload distortion or the slope-overload error***. Thus, slope-overload error occurs when the slope of $x(t)$ is much higher than $x_q(t)$.  Fig. Illustrating the phenomenon of slope overload in linear delta modulation	2M

		GRANULAR NOISE: • When the input signal *x(t)* is relatively constant in amplitude with time, the approximated signal $x_q(t)$ will *hunt* above and below *x(t)* as shown in Figure. This leads to a noise called ***granular noise***. • It increases with increase in step size δ. To reduce granular noise, the step size should be as small as possible. However, this will increase slope-overload distortion.  Fig. Granular noise	2M
	c)	**Describe natural sampling with neat sketch.**	4M
	Ans:	**1. Natural Sampling or Chopper Sampling**	1M
		Natural Sampling is a practical method of sampling in which pulse have finite width equal to T. Sampling is done in accordance with the carrier signal which is digital in nature.  With the help of functional diagram of a Natural sampler, a sampled signal g(t) is obtained by multiplication of sampling function c(t) and the input signal x(t). Spectrum of Natural Sampled Signal is given by: $G(f) = A\tau/ T_s .[\Sigma \sin c(n f_s.\tau) X(f-n f_s)]$	2M
		Natural Sampled Waveform	1M



d) **Describe generation of BASK signal with the help of block diagram** **4M**

Ans: **2M**



ASK Transmitter

-

OR

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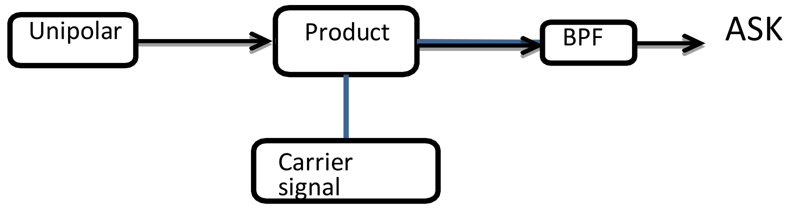
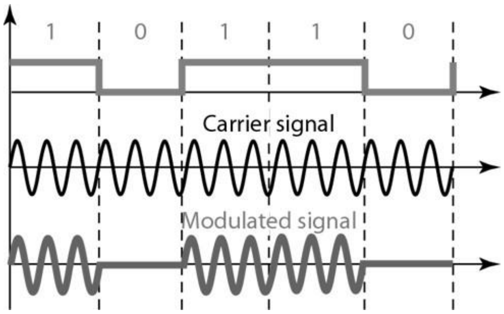


Explanation of ASK Transmitter

- The ASK technique of binary modulation is illustrated in Figure where modulating signal consists of unipolar pulses. **1M**
- Because in this case the carrier is switched ON and OFF, this method is also known as *ON-OFF keying*.
- For the entire time the binary input is high, the output is a constant amplitude, constant frequency signal and for the entire time the binary input is low, the carrier is off.
- Ps is signal power given by (Amplitude) ^{2} /2
- ASK is given by:
- $v_{ASK}(t) = b(t) \sin\omega_c t$

WAVEFORM:



1M

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Q. No.	Sub Q. N.	Answers	Marking Scheme
3		**Attempt any THREE of the following :**	**12-Total Marks**
	a)	**Explain any one method of error detection with example.**	**4M**
	Ans:	Duplicating each data unit for the purpose of detecting errors is a form of error detection called *redundancy.* Adding bits for the purpose of detecting errors is called *redundancy checking.* There are four basic types of redundancy checks: **1. Vertical Redundancy Checking (VRC)** **2. Checksum** **3. Longitudinal Redundancy Checking (LRC)** **4. Cyclic Redundancy Checking (CRC)** **METHOD 1:** **VERTICAL REDUNDANCY CHECKING (VRC):** ● *Vertical Redundancy Checking (VRC)* is the simplest error detection scheme and is generally referred to as *Character parity* or simply *Parity.* With character parity, each character has its own error detection bit called the parity bit. Since the parity bit is not actually a part of the character, it is considered as a redundant bit. ● An "n" *character* message would have n redundant parity bits. Therefore, the number of Error detection bits are directly proportional to the length of the message. ● Parity can be of two types: 1. Odd parity 2. Even parity In *odd parity,* the total number of 1's in the entire message should be odd whereas in *even parity,* the total number of 1's in the message should be even. ● With character parity (VRC), a single parity bit is added to each character to force the total Number of logic 1's in the character, including the parity bit, to be either an odd number (odd parity) or an even number (even parity). ● For example, the ASCII code for the letter C is 43H or P1000011, where the P bit is the parity bit. There are three logic 1's in this code, not counting the parity bit. ● If *odd parity* is used, the P bit is made logic 0, keeping the total number of logic 1's at three, which is an odd number. ● If *even parity* is used, the P bit is made logic 1, making the total number of logic 1's four, which is an even number. ● The main advantage of parity is its simplicity.	**Any one method Explanation = 2M, Example =2M**

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OR

METHOD 2:

LONGITUDINAL REDUNDANCY CHECKING (LRC):

● Longitudinal Redundancy Checking (LRC) is a redundancy error detection scheme that uses parity to determine if a transmission error has occurred within a message and is therefore Sometimes called *message parity.*

● With LRC, each bit position has a parity bit. In other words, b_0 from each character in the Message is XOR'ed with b_0 of all the other characters in the message. Similarly, b_1 , b_2 and so on are XOR'ed with their respective bits from all the characters in the message. Essentially, LRC is the result of XORing the "character codes" that make up the message, whereas VRC is the XORing of the bits within a single character.

● With LRC, even parity is generally used, whereas with VRC, odd parity is generally used. The LRC bits are computed in the transmitter while the data are being sent and then appended to the end of the message as a redundant character.

● In the receiver, the LRC is recomputed from the data and the recomputed LRC is compared to the LRC appended to the message. If the two LRC characters are the same, most likely no Transmission errors have occurred. If they are different, one or more transmission errors have occurred.

● Let us take an example to show how VRC and LRC **(two dimensional parity checking)** are calculated and how they can be used together

Example: Determine the VRC and LRC for the following ASCII encoded message: THE CAT. Use odd parity for the VRC and even parity for the LRC.

Solution:

Character	Bit position	T	H	E	space	C	A	T	**Parity Bits LRC**
ASCII Code	B_1	0	0	1	0	1	1	0	1
	B_2	0	0	0	0	1	0	0	1
	B_3	1	0	1	0	0	0	1	1
	B_4	0	1	0	0	0	0	0	1
	B_5	1	0	0	0	0	0	1	0
	B_6	0	0	0	1	0	0	0	1
	B_7	1	1	1	0	1	1	1	0
Parity Bit (VRC)	B_8	0	1	0	0	0	1	0	0

The LRC is 00101111 (2FH)

VRC and LRC are together called two dimensional parity check.

OR

METHOD 3:

CHECKSUM:

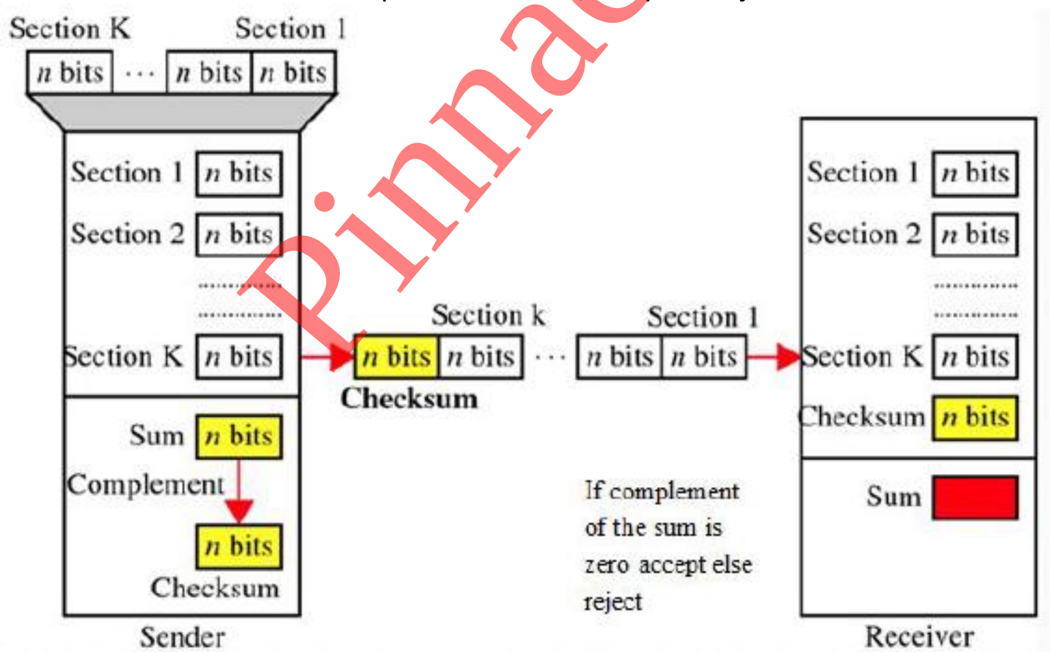
Checksum is error detection method which is based on the concept of redundancy. The checksum detects all errors involving an odd number of bits and most errors involving an even number of bits.

● Checksum encoder follows the following steps

1. The data unit is divided in to "k" sections each of "n" bits
2. All sections are added to get the sum.
3. The sum is complemented and becomes the checksum.
4. The checksum is send as redundant bits along with the data.

● Checksum decoder/checker follows the following steps

1. The data unit is divided in to "k" sections each of "n" bits
2. All sections are added to get the sum.
3. The sum is complemented.
4. If the result is zero data are accepted otherwise; They are rejected.



● For example suppose the following block of 16 bits is to be sent using a checksum of 8 bits

● 10101001 00111001

● The number are added using one's complement arithmetic

Data unit 1	10101001
Data unit 2	00111001
sum	11100010
one's complement (checksum)	00011101

- pattern sent is ← 10101001 00111001 00011101
- Suppose receiver receives the pattern without any error
- 10101001 00111001 00011101
- the receiver adds the three sections it will get sum as all one's which after complimenting is all zero's and shows that there is no error

Data unit 1	10101001
Data unit 2	00111001
one's complement (checksum)	00011101
sum	11111111
complement of sum	00000000

- If the complement of the sum is zero means the pattern is received without error.

OR

METHOD 4:-

Cyclic redundancy check:

CRC is very effective error detection method. It can detect burst errors that affect odd number of bits. Burst error of length less than or equal to the degree of polynomial. CRC is based on binary division. In CRC a sequence of redundant bits called as CRC remainder is appended to the end of the data unit so that the resulting data unit becomes exactly divisible by a second predetermined binary number. At the destination the incoming data unit is divided by the same number (divisor) if at this step there is no remainder the data unit is assumed to be intact and therefore accepted. If the remainder is non zero then the data unit is discarded.

For example data is 100100 and divisor is 1101:

At the transmitter ends.

● String of n zero's is appended to the data unit. The number "n" is 1 less than the number of bits in the predetermined divisor, which is n+ 1 bit.

● The newly elongated data unit is divided by the divisor using binary division. The remainder resulting from this division is the CRC.

- Now the CRC of "n" bits derived from step 2 replaces the appended 0's at the end of the data unit.CRC may consists of all 0's.
- Send the data unit with CRC.

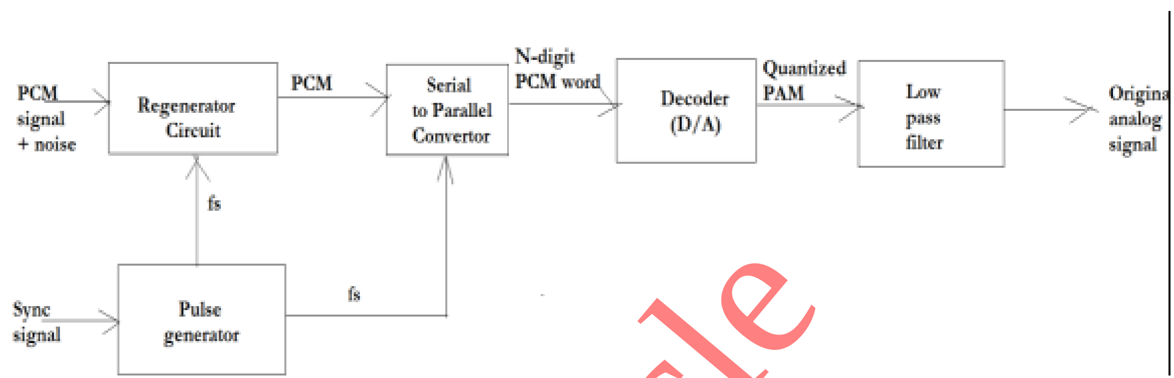
```
                 1 1 1 1 0 1      quotient
        ------------------------------------------
1 1 0 1        | 1 0 0 1 0 0 0 0 0  (data plus extra 3 zero)
divisor        | 1 1 0 1
               | ----------------
               |   1 0 0 0
               |   1 1 0 1
               | --------------------
               |     1 0 1 0
               |     1 1 0 1
               | ----------------------
               |       1 1 1 0
               |       1 1 0 1
               | ------------------------
               |         0 1 1 0
               |         0 0 0 0
               | --------------------------
               |           1 1 0 0
               |           1 1 0 1
               | ----------------------------
               |             0 0 1   remainder
```

At the receiver ends.

- The data unit followed by CRC arrives at the receiver.
- Receiver treats whole string as a unit and divides it by the same divisor.
- If the string arrives without error, the CRC checker yields a remainder of zero and the data unit is accepted. If some errors occur during transmission, CRC will be non zero and the data is accepted.

```
                 1 1 1 1 0 1      quotient
        ------------------------------------------
1 1 0 1        | 1 0 0 1 0 0 0 0 1  (data plus CRC received)
divisor        | 1 1 0 1
               | ----------------
               |   1 0 0 0
               |   1 1 0 1
               | --------------------
               |     1 0 1 0
               |     1 1 0 1
               | ----------------------
               |       1 1 1 0
               |       1 1 0 1
               | ------------------------
               |         0 1 1 0
               |         0 0 0 0
               | --------------------------
               |           1 1 0 1
               |           1 1 0 1
               | ----------------------------
               |             0 0 0   result
```

<table>
<tr><td></td><td></td><td>Since the remainder is zero, drop the CRC and accept the data.</td><td></td></tr>
<tr><td></td><td>b)</td><td>Draw the block diagram of PCM receiver with the help of relevant wave form and explain its working</td><td>4M</td></tr>
<tr><td></td><td>Ans:</td><td>Block diagram of PCM receiver:-



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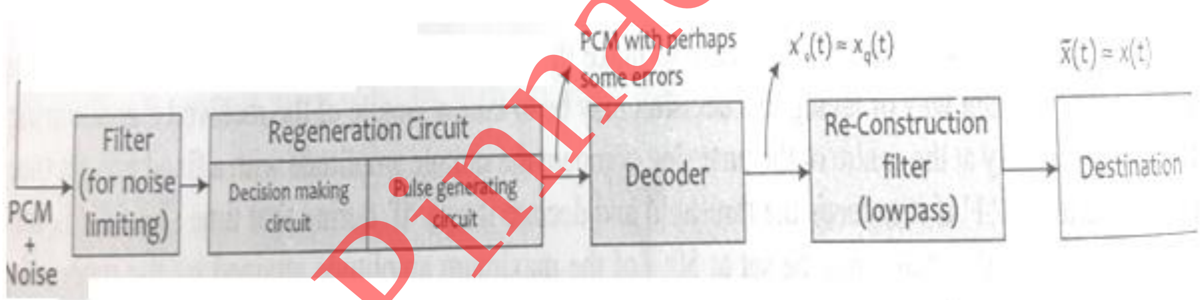

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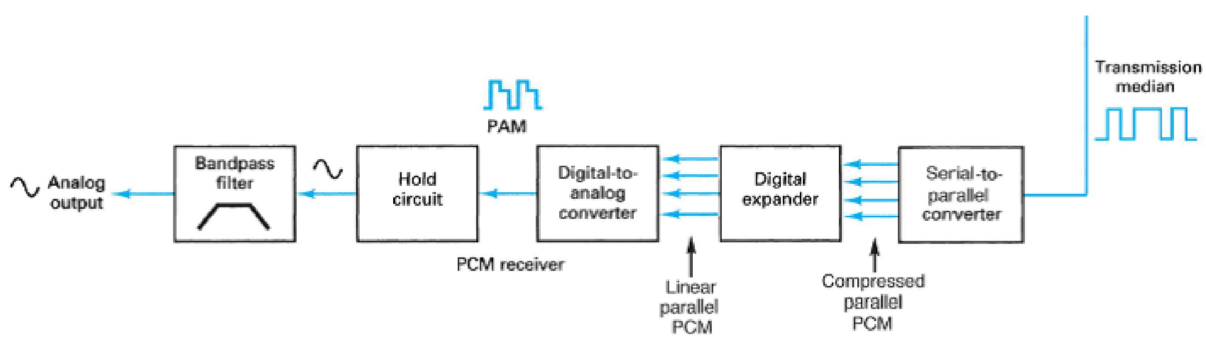
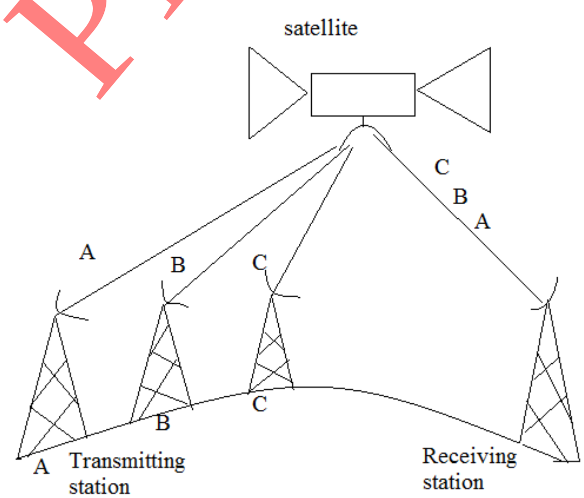


Explanation:-

A PCM signal contaminated with noise is available at the receive input.
The regeneration circuit at the receiver will separate PCM pulses from noise and will reconstruct original PCM signal.
</td><td>Any one correct diagram with Waveform at each block = 2M, Explanation = 1M, Waveform 1M)</td></tr>
</table>

		• The pulse generator has to operate in synchronization with that at transmitter. • Cleaned PCM is fed to a serial to parallel converter. • Then applied to a decoder which converts each code word into corresponding quantized sample value. This quantized PAM signal is passed through a low pass filter recovers the analog signal x (t).	
	c)	**Draw the block diagram of TDMA system and explain its working.**	**4M**
	Ans:	**Block diagram of TDMA system:-**  **OR**  **Explanation:-** • In TDMA, each user has all the bandwidth, all the power and part of the time. It is frequently used with data and digital voice transmission. TDMA sends data in buffer and	**Block diagram =2M, Explanation = 2M**

hence it is bursty communication. It is non-continuous. TDMA cannot send an analog signal directly due to buffering required. It is used for digital data.

- In this method, all the earth stations share transponder time. Each earth station in the network is allocated a time slot in a periodic sequence.
- It is a method of time division multiplexing, digitally modulated carrier between participating earth stations within the satellite network through a common satellite transponder. With TDMA, each earth station transmits a short burst of digitally modulated carrier during a precise time slot (called ***epoch***) within a TDMA frame.
- Each earth station's burst is synchronized so that it arrives at the satellite transponder at a different time. Consequently, only one earth station's carrier is present in the transponder at any given time thus avoiding collision with another station's carrier.
- The transponder is an RF to RF repeater that simply receives the earth stations transmissions, amplifies them and retransmits them in a downlink beam that is received by all participating earth stations. Each earth station receives the bursts from all other earth stations and must select from them the traffic destined only for itself.

d) **Compare TDMA and CDMA on the basis of sharing of time and B.W. Synchronization, code word ,guard band and guard time.** **4M**

Ans: **1M each Point**

Sr. No	Parameters	TDMA	CDMA
1	**Sharing of time & B.W**	Sharing of time of satellite Transponder using entire BW	Sharing of time and bandwidth both.
2	**Synchronization**	Time synchronization is essential.	Code Synchronization is required.
3	**Code Word**	No code word is required	Code words are required by ground stations.
4	**Guard band and guard time**	Guard times are required	Both guard times and guard bands are required if it uses along with TDMA & FDMA. Otherwise not required.

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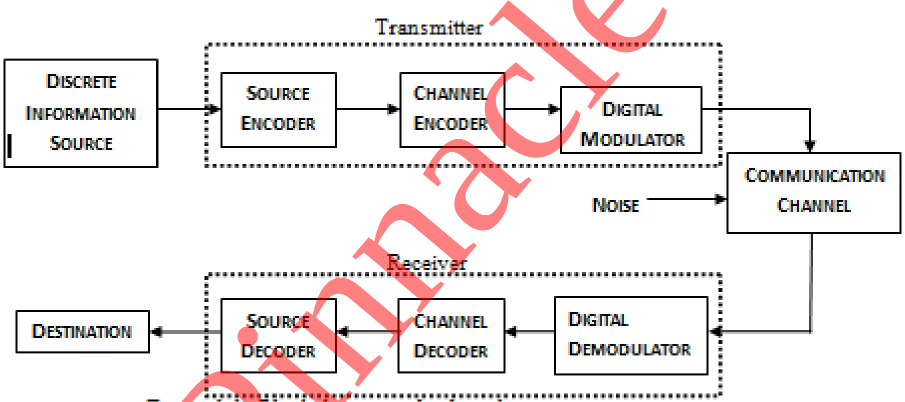
4		**Attempt any THREE of the following :**	**12-Total Marks**
	(a)	**Explain digital communication system with the help of block diagram.**	**4M**
	Ans:		**Block diagram= 2M, Explanation = 2M**

Block diagram of digital communication system:-



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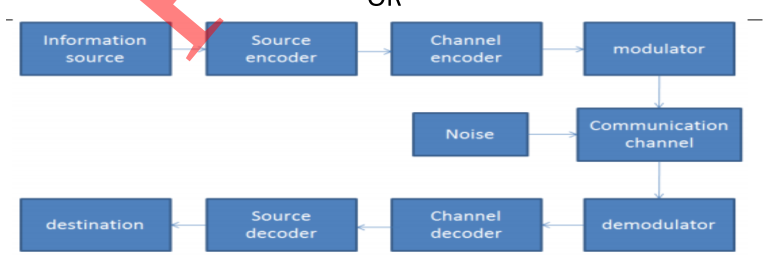

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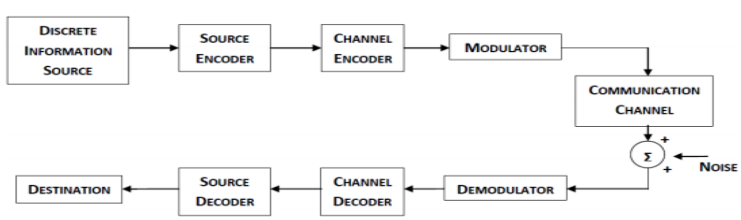


Explanation:-

DISCRETE INFORMATION SOURCE:

- The information to be transmitted originates here. These information/messages may be available in digital form or it may be available in an analog form.
- If it is analog it is sampled and digitized using an A/D converter to make the final source output to be digital in form.

SOURCE ENCODER :

- The source encoder therefore reduces the redundancy by performing a one to one mapping of its input bit stream in to another bit stream at its output, but with fewer digits.
- Thus in a way it performs data compression.

CHANNEL ENCODER:

- The channel encoder is intended to introduce controlled redundancy into the bit stream at its input in order to provide some amount of error- correction capability to the data being transmitted.

DIGITAL MODULATOR:

- The physical channels are basically analog in nature; the digital modulator takes each digital binary digit at its input and maps it, in a one –to – one fashion, into a continuous waveform.
- Binary 'zero' at its input is mapped into a continuous signal $s_0(t)$ and binary 'one' is mapped into another continuous signal $s_1(t)$.
- This is called binary modulation.

PHYSICAL CHANNEL:

- The digitally modulated signal is passed on to the physical channel, which is nothing but the physical medium through which the signals are transmitted.
- It may take a variety of forms- a pair of twisted wires, coaxial cable, a wave guide, a microwave radio, or an optical fiber.

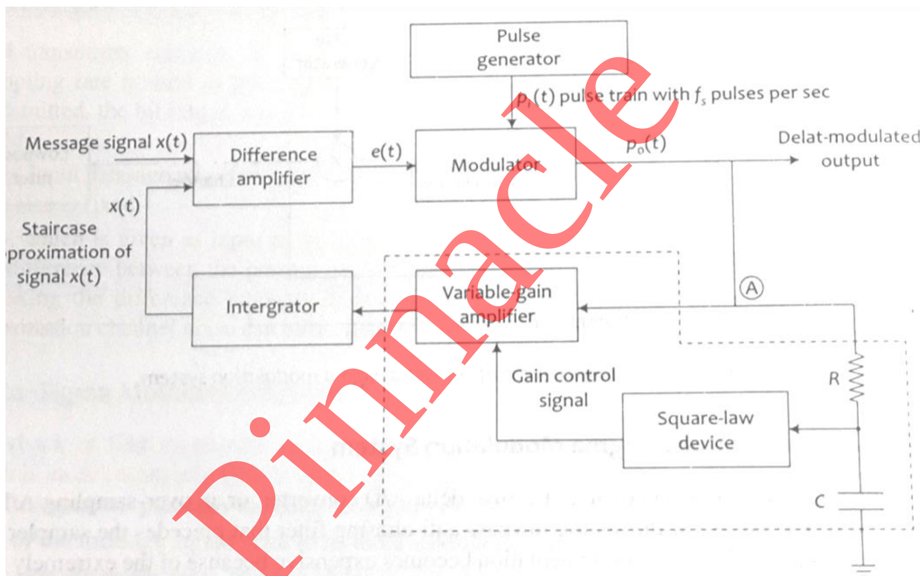
THE DIGITAL DEMODULATOR:

- The digital demodulator of the receiver receives the noise corrupted sequence of waveforms from the channel and by inverse mapping tries to give at its output, an estimate of the sequence of the binary digits that were available at the input of the digital modulator at the transmitting end.

THE CHANNEL DECODER:

- The output sequences of digits from the digital demodulator are fed to the channel decoder. Using its knowledge of the type of coding performed by the channel encoder at the transmitting end and using the redundancy introduced by the

<table>
<tr><td></td><td></td><td>channel encoder, it produces as its output, the output of the source coder of the transmitter with as few errors as possible.
<u>THE SOURCE DECODER:</u>
• Using its knowledge of the type of encoding performed by the source encoder of the transmitter, the source decoder of the receiver tries to reproduce at its output, a replica of the output of the digital source at the transmitting end.</td><td></td></tr>
<tr><td></td><td>(b)</td><td>Describe the working of an ADM transmitter with neat block diagram.</td><td>4M</td></tr>
<tr><td></td><td>Ans:</td><td>ADM transmitter Block diagram:-



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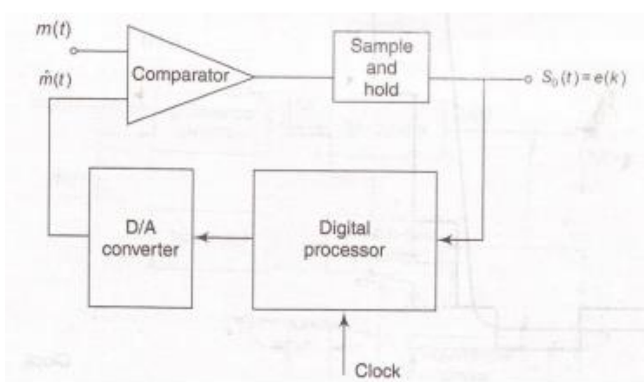
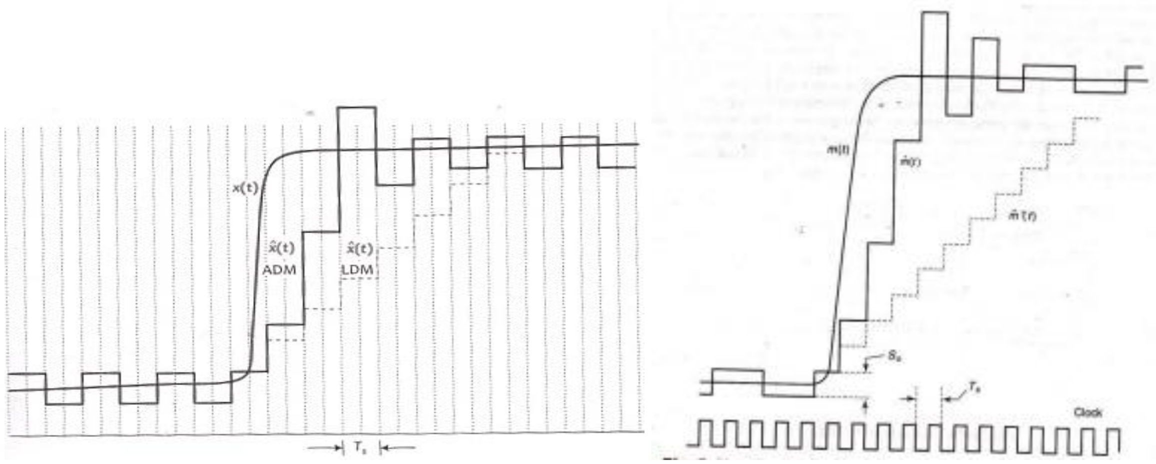


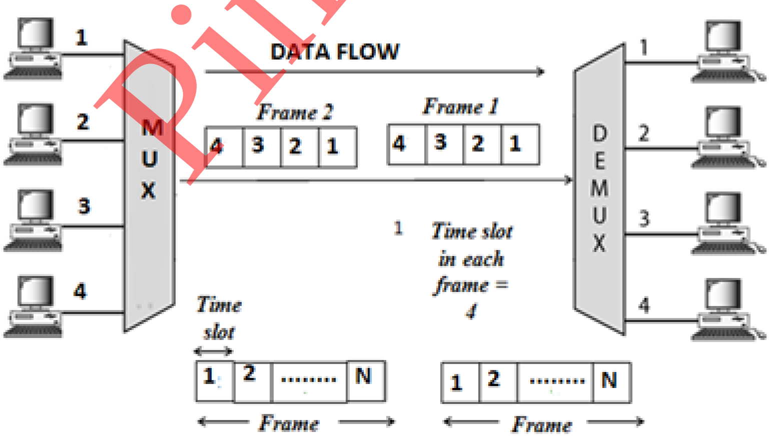
</td><td>(Block diagram = 2M, Working =2M)</td></tr>
</table>



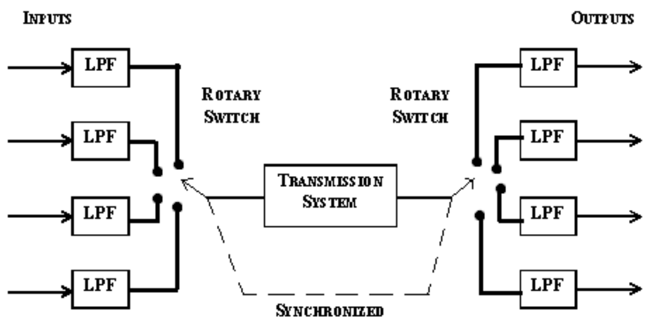
(Waveform is optional)

Working:-

- A DM system that adjusts its step size according to the information signal characteristics is called as Adaptive Delta Modulation (ADM). Here the step size is not constant. The block diagram for generation of ADM signal is shown in above Figure
- The step size δ is varied by controlling the variable-gain amplifier which is assumed to have a low gain when the control voltage is zero and a large gain when the control voltage increases. The gain-control circuit consists of an *RC* integrator and a square-law device.
- Pulse generator produces narrow pulses of fixed amplitude at a rate equal to the desired sampling rate. The modulator consists of hard limiter and a product device/multiplier.
- Whatever be the actual value of e(t) the hard limiter output will be +1 if e(t) is positive and -1 if e(t) is negative. So the polarity of $p_o(t)$ depends on the sign of e(t).
- The subsystem within a dotted line box is for adaptation.
- When the input signal is constant or slowly varying, DM signal will be hunting and the modulator output will be a sequence of alternate polarity pulses, there will not be any charge on the capacitor and the voltage across it will be zero.
- So the gain control is voltage is almost zero and there will not be any change in the amplitude of the pulses at the output of the variable gain amplifier. As the gain of this amplifier is adjusted initially to be low when the gain control voltage level is zero we have thus ensured that the step size is small when x (t) is almost constant or changing very slowly and thus, granular noise is reduced as shown in above Figure
- Now if x (t) is steeply rising or falling for some time the consecutive pulses in the pulse train will either be all positive or all negative. So the capacitor will be charged

		irrespective of whether it is positively charged or negatively. • Due to the squaring device (square law device), the amplifier gain will be increased no matter what the polarity of the capacitor voltage is. The net result is an increase in step size and a reduction in slope-overload distortion as shown in figure	
	(c)	**Explain TDM technique with relevant diagram.**	**4M**
	Ans:	**TIME DIVISION MULTIPLEXING (TDM):** • TDM is a digital multiplexing technique in which many signals are transmitted for very short time (time slot) over common transmission channel. Here each signal can utilize the entire bandwidth of the channel. Figure 5.6 illustrates the concept of TDM. • Here each signal will be transmitted for a short duration of time. One cycle or frame is said to be complete when each time slot is dedicated to each signal. With n input signals (transmitting devices), each frame has n time slots, with each slot allocated for carrying data from a specified device. • The TDM signal in the form of frames is transmitted on the common communication medium. TDM can be used to multiplex analog or digital signals but it is suitable for digital signal multiplexing.  *Conceptual Diagram of TDM* **OR** **BLOCK DIAGRAM OF TDM SYSTEM:** • TDM is a digital multiplexing process that can be applied when the data capacity of the transmission medium is greater than the data rate required by the transmitting and receiving devices. In such cases, multiple transmissions can occupy a single link	**(Block diagram = 2M, Working =2M)**

by subdividing them and interleaving the portions. Figure 5.7 shows the block diagram of TDM system consisting of four channels.



Block Diagram of a four channel TDM System

TDM TRANSMITTER:

- Four input signals, all band-limited to f_x by the input filters (LPF) are sequentially sampled at the transmitter by the *rotary switch or commutator*. The switch makes f_s revolutions per second and extracts one sample from each input during each revolution.
- The output of the switch is a PAM waveform containing samples of the input signals periodically interlaced in time. The samples from adjacent input message channels are separated by T_s/M where M is the number of input channels.
- A set of M pulses containing one sample from each of the M input channels is called a ***frame***.

TDM RECEIVER:

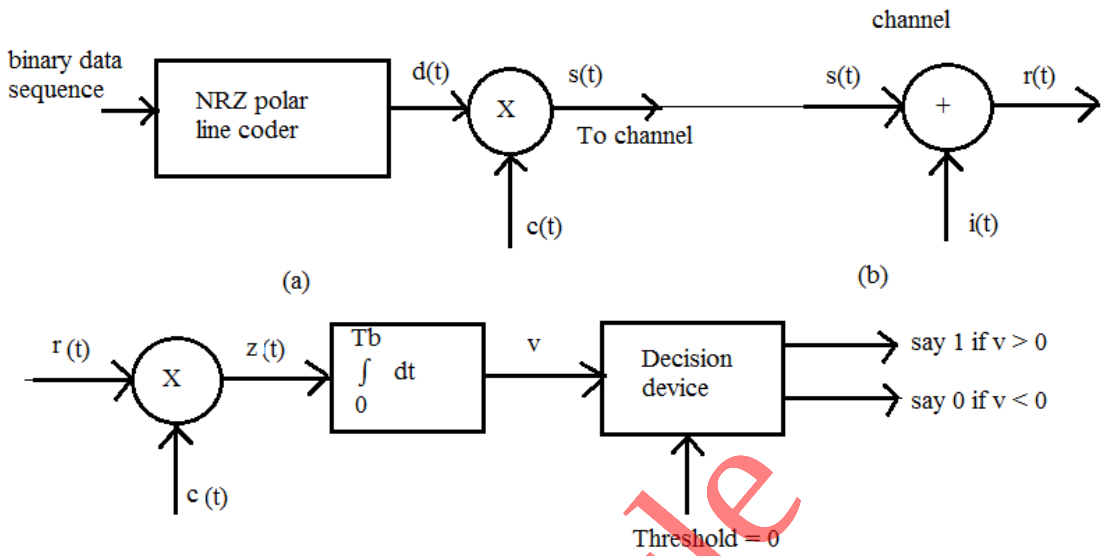
- At the receiver, the samples from the channel are separated and distributed by another rotary switch called as a *distributor* or *de-commutator*.
- The samples from each channel are filtered to produce the original message signal. The rotary switches at the transmitter and receiver are usually electronic circuits that are carefully synchronized. There are two levels of synchronization in TDM:

1. Frame Synchronization
2. Sample (or word) synchronization

- *Frame synchronization* is necessary to establish the beginning of each frame and *sample (or word) synchronization* is necessary to properly separate the samples within each frame.

	(d)	**Explain with the help of block diagram, spread spectrum modulation system.**	**4M**

Ans: **SPREAD-SPECTRUM COMUNICATION SYSTEM**



Baseband DS spread spectrum communication system model (a)transmitter (b) channel (c)receiver

Block diagram = 2M, Explanation =2M)

Explanation:-

- In actual DSSS system, the binary data to be transmitted is first carrier modulated using PSK and then this modulated signal is subjected to spreading by multiplying it by the PN sequence. However, in order to discuss the effect of multiplying the data sequence by the PN sequence, for the present we shall consider only a base band signal.
- Let the data sequence be denoted by d(t) and the PN sequence be denoted by c(t). Let the data duration be T_b sec and PN sequence duration be T_c sec. In DSSS it is always so arranged that $T_c << T_b$
- The wave form d(t) is a narrow band signal, while the c(t) wave form is a wide band signal. The product wave form s(t) will have spectrum which is almost like spectrum of c(t), the PN sequence.
- In order to illustrate how the spread – spectrum modulation enables us to reject the deterministic interfering signals added to the transmitted signal s(t) during the course of its passage through the channel, we are adding the interfering signal i(t) to the DSSS signal s(t).

Since the interference is additive

$$r(t) = s(t) + i(t)$$

$$r(t) = d(t).c(t) + i(t)$$

- The first operation to be performed at the receiver is to de-spread the received signal. For this purpose, it is multiplied by the PN sequence waveform c (t), which is assumed to be in perfect synchronism with the c(t) used at the transmitter side.

$$Z(t) = r(t).c(t)$$

$$Z(t) = d(t).c_2(t) + i(t).\ c(t)$$

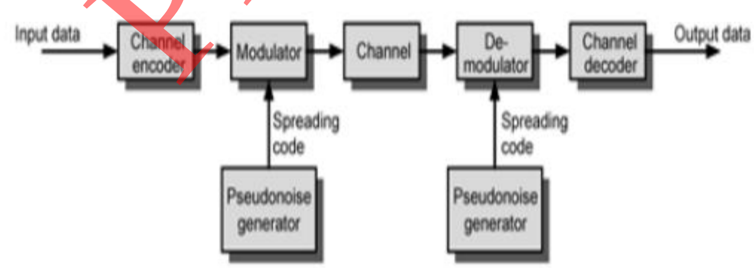
C(t) is either 1 or -1 at any time

Hence $c_2(t)$ = 1 always

$$Z(t) = d(t) + i(t).\ c(t)$$

- We find that when we de-spread the message or data waveform d(t), the interference signal is spread over a wide bandwidth by getting multiplied by the PN sequence waveform c(t).
- Thus we find that z(t) consists of a narrow band component d(t) and a wide band component i(t).c(t).
- Z(t) is integrated over a period of T_b , data bit duration. The integrator acts as a low pass filter and removes the wide band component thus achieving suppression of the interfering signal.
- The output of the integrator gives a voltage v, whose value depend on whether the d(t) was +1 or -1 during interval T_b .
- This voltage is given to the comparator which acts as the decision device and says that d(t) was 1 during that Tb if v>0 and that it was a -1 if v<0.

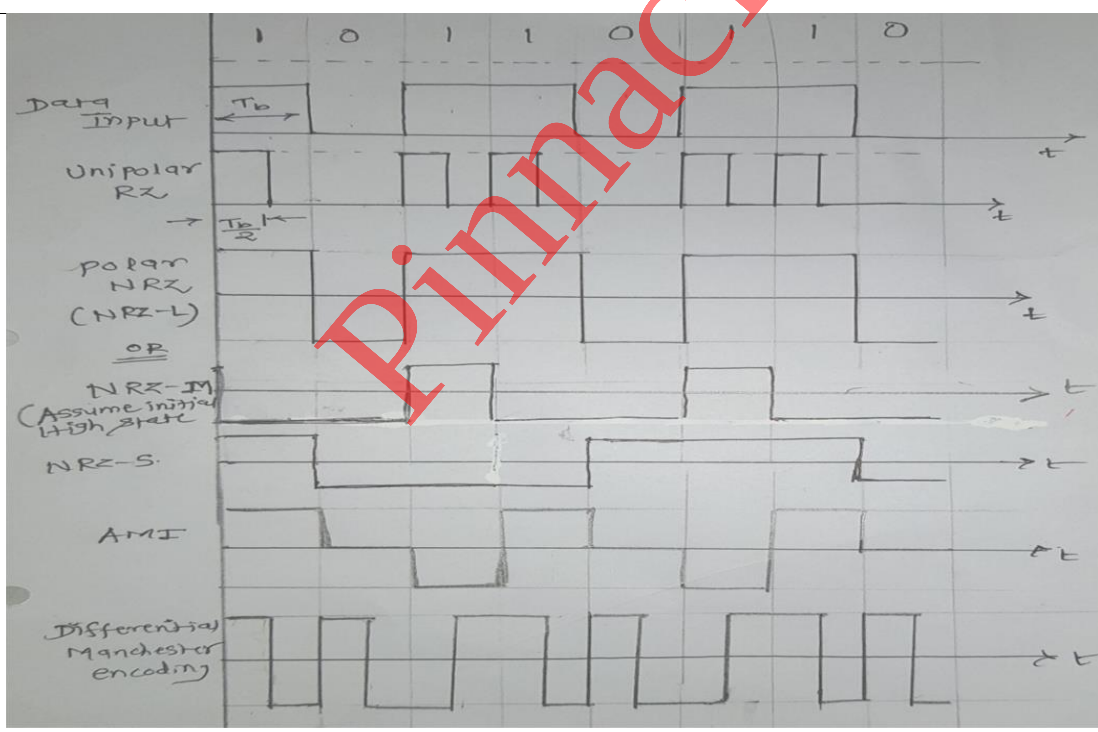
OR



General Model of a Spread Spectrum system

Explanation Of Spread Spectrum Modulation System:-

1. Basic elements of a spread spectrum signal modulation system is shown below.
2. Channel encoder adds extra bits to the information binary sequence for error detection & correction purpose.

		3. PN sequence generation at the transmitter & receiver generates identical PN binary valued sequence 4. PN sequence is impressed on the information signal at the modulator (Tx) and remove from the received signal at the Demodulator. 5. Synchronization of the PN sequence generator at the receiver with the PN sequence contained in the incoming received signal is required in order to demodulate the received signal. Prior to the transmission of information Synchronization may be achieved by transmitting a fixed PN sequence pattern which the receiver will recognize in the presence of interference with high probability.	
	(e)	**Encode binary sequence 10110110 using unipolar-RZ ,polar-NRZ,AMI and differential Manchester line coding techniques**	**4M**
	Ans:		**1M each**

Q. No.	Sub Q. N.	Answers	Marking Schem

SUMMER-19 EXAMINATION

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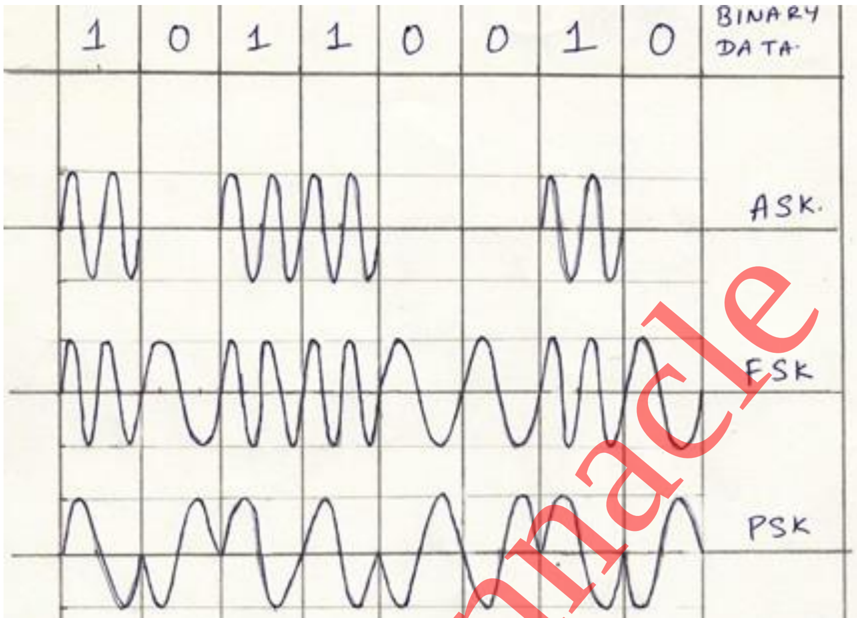
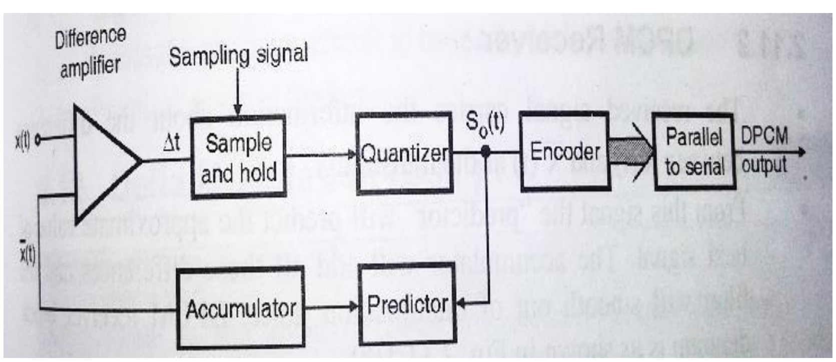
			e
5.		**Attempt any TWO of the following:**	**12-Total Marks**
	a)	**Generate CRC code for data word 1101101001 by using divisor as 1101. State two advantages of CRC method.**	**6M**
	Ans:	Data word - 1101101001 Divisor - 1101 length of divisor = n bits = 4 bits Dividend = Data word appended by (n-1) zeros here n-1 = 4-1 = 3 Dividend = 1101101001000 Carry out division for CRC generation  CRC Code word = Data word appended by CRC bits. so CRC code word = 1101101001001 Advantages of CRC Code: 1. CRC codes are capable of detecting any kind of error brust. 2. CRC can detect all brust errors of length less than or equal to degree of polynomial. 3. implementation of encoding and error detection circuit is possible practically.	**Correct division 3M & Correct CRC Code 1M** **ANY 2 ADVANTAGES 2M**
	b)	**State BW required for BASK, BFSK and BPSK, Also draw waveforms for binary data 10110010 in ASK,FSK,PSK modulation.**	**6M**

	Ans:	**Bandwidth requirements of:** • **BASK = 2fb** • **BFSK = 4fb** • **BPSK = 2fb** 	3M Bandwidth requirements 1M 1M 1M
	c)	**Justify that in DPCM system, less number of bits are transmitted than PCM system with the help of block diagram and relevant waveform.**	6M
	Ans:	 **block diagram of DPCM system**	3M

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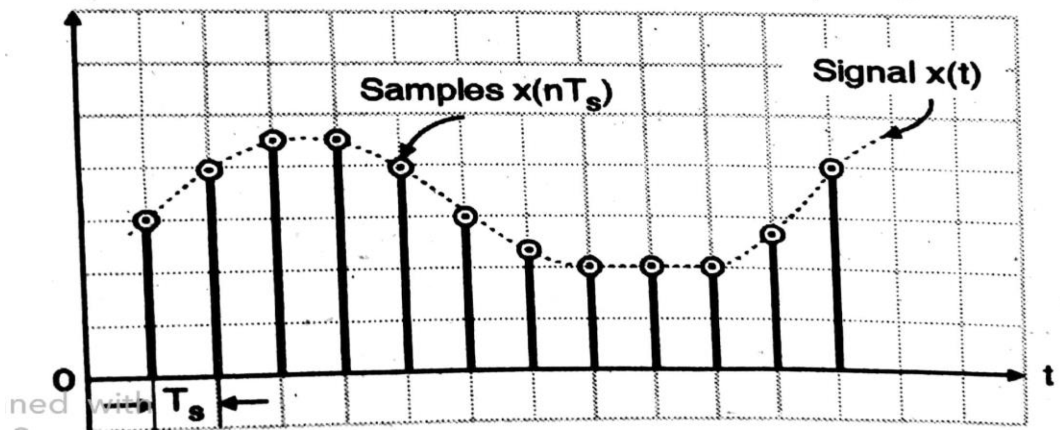
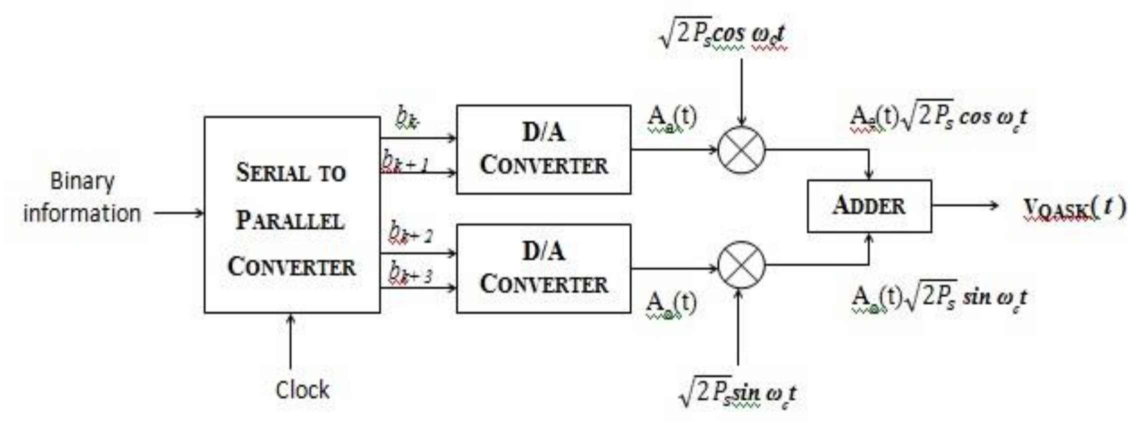
		 **Fig:Samples have a correlation between them** **It is observed that if the sampling takes place at a rate which is higher than the Nyquist rate, then there is a correlation between successive samples of the signal x(t).** **Hence we can predict the range of next required increment or decrement in x(t) at the predictor output, if we know the past sample value or the difference.** **This reduces the difference between x(t) and x^(t).therefore to encode this small value of error the DPCM system requires less number of bits per sample which will ultimately reduce the bandwidth requirement.** **It shows that in DPCM system, less number of bits/sample are transmitted than PCM system**	1M **2M**

Q. No.	Sub Q. N.	Answers	Marking Scheme
6.		**Attempt any TWO of the following :**	**12-Total Marks**
	a)	**Draw the neat block diagram of QAM system , explain its working.**	**6M**

Ans:



Explanation:

- The bit stream b(t) is applied to the serial to parallel converter, operating on a clock which has a period of T_s, which is the symbol duration. The bits b(t) are stored by the converter and then presented in the parallel form. The four bit symbols are b_{k+3}, b_{k+2}, b_{k+1}, b_k.
- Out of these four bits, the first two bits are applied to a D/A converter and the other two bits are applied to the second D/A converter.
- The output of the first converter is $A_e(t)$, which is modulated by the carrier $\cos\omega_c t$ whereas the output of the second D/A converter, $A_o(t)$ is modulated by the carrier $\sin\omega_c t$ in the balanced modulators.
- $A_e(t)$,$A_o(t)$are voltage levels generated by the convertor -3,-1,+1,+3 volts.
- The balanced modulator outputs are added together to get the QAM output signal which is expressed as,

$$v_{QASK}(t) = A_e(t)\cos\omega_c t + A_o(t)\sin\omega_c t$$

(any relevant diagram can consider)

Explanation: 3M, Block diagram :3 M,

b) **Describe the M-ary PSK encoding technique with neat block diagram and also draw constellation diagram of BPSK, QPSK.** — 6M

Ans: **M-ary PSK encoder:** — 2M

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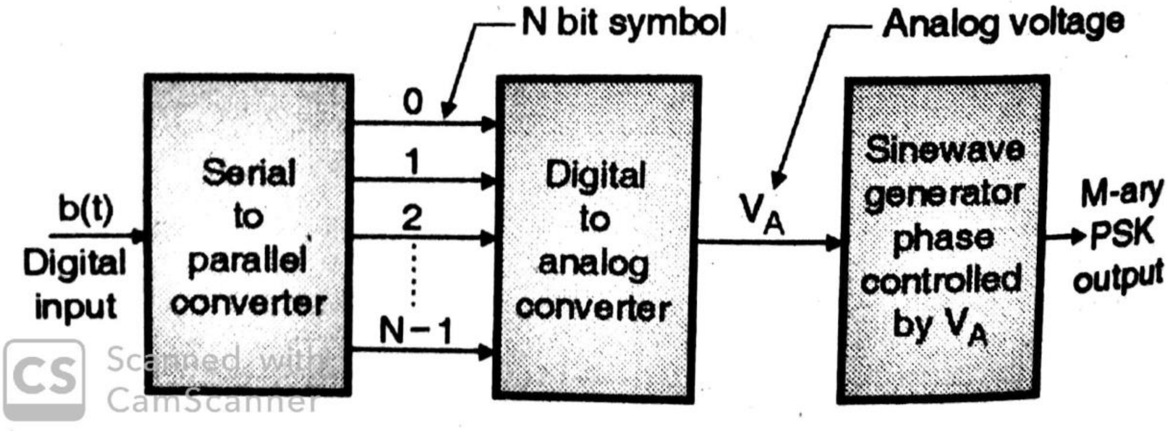
Subject Name: Digital Communication System Model Answer Subject Code: 22428



2M

Working:

1) The bit stream b (t) is applied to a serial to parallel converter. This block can store the N bits of a symbol

2) These N bits per symbol appear serially, in the form of a sequence one after the other

3) The N bits per symbol are first assembled by the serial to parallel converter block. Then all these bits are presented simultaneously (in the parallel form) on the N output lines of the converter. Thus N bits message appears in the parallel form at the output of the serial to parallel converter.

4) The output of the serial to parallel converter remains unchanged for a duration of NT_b of a symbol. This time duration is used by the converter to assemble a new group of N bits.

5) After every NT_b seconds, the converter output changes to a new N bit symbol.

6) The N bit output of the converter is then applied to a D/A converter. The N bit digital input, is converted in to an analog output V_A

7) The N bit digital input can have 2^N= M number of possible combinations. Therefore the D/A converter output V_A will have M number of distinct values, corresponding to the M symbols.

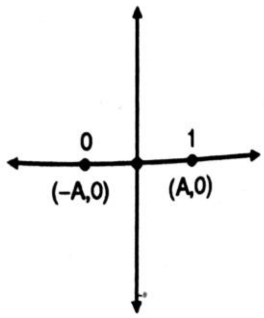
8) Finally this analog voltage is applied to a sinusoidal signal generator, which produces a constant amplitude sinusoidal output voltage, the phase ϕ_m of which is proportional to

the D/A converter output V_A

9) Thus at the output of the transmitter, we get a fixed amplitude sinusoidal waveform, the phase of which has a one to one correspondence to the N bit symbols.

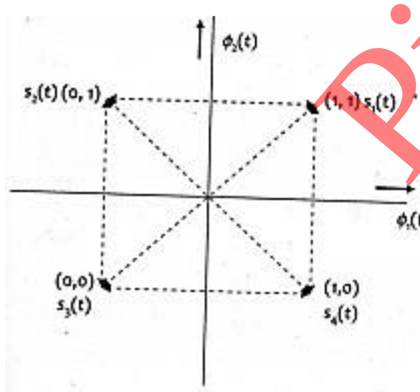
10) The phase will change only once per symbol time $T_s = N\ T_b$ Thus the M-ary PSK is generated. **1M**

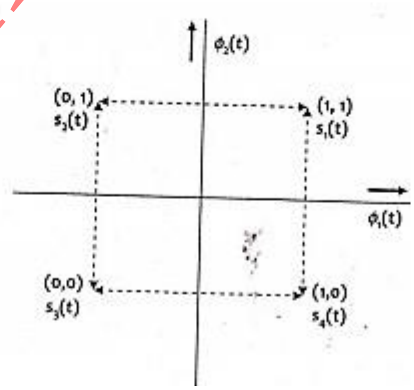
CONSTELLATION DIAGRAM



CONSTELLATION DIAGRAM BPSK **1M**

CONSTELLATION DIAGRAM FOR QPSK (ANY ONE)





OR

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Subject Name: Digital Communication System Model Answer Subject Code: 22428

			
	c)	**Differentiate between direct sequence spread spectrum and frequency hopped spread spectrum.**	**6M**

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Subject Name: Digital Communication System **Model Answer** **Subject Code:** 22428

Ans:

DSSS	FHSS
• Definition: PN sequence of large bandwidth is multiplied with a narrow band information signal.	• Definition: Data bits are transmitted in different frequency slots which are changed by PN sequence.
• Chip rate $(R_c) = \frac{1}{Tc}$	• Chip rate $(R_c) = max(R_b, R_s)$
• Applications with large multipath delays: DS represents a reliable mitigation method as such signals render all multipath signal copies that are delayed by more than one chip time from direct signal as invisible to the receiver.	• FH systems can provide the same mitigation only if the hopping rate is faster than the symbol rate and if the hopping bandwidth is larger.
• For commercial applications implementation of DSSS radios with large gap can also be costly due to the need of high speed circuits.	• Implementation of FHSS radio can be costly and complex due to the need of high speed frequency synthesizers.
• DSSS radios encounter more randomly distributed errors that are continuous and lower level.	• SFH suffers from strong burst error.
• Modulation technique: BPSK.	• Modulation technique: M-ary FSK
• Long acquisition time.	• Short acquisition time.
• DSSS is distance dependent.	• In FHSS, effect of distance is less.
• Processing gain is less.	• Processing gain is higher.
• Bandwidth required is less than FHSS system.	• Bandwidth of FHSS system is too high.

Any 6 points 6M